AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-36. (canceled).

37. (previously presented): A n-type group III nitride semiconductor layered structure comprising a substrate and, stacked on the substrate, an n-type impurity concentration periodic variation layer comprising an n-type impurity atom higher concentration layer and an n-type impurity atom lower concentration layer, said n-type impurity atom being Ge, pits being provided on a surface of the higher concentration layer (a surface remote from the substrate), and said lower concentration layer being stacked on said higher concentration layer, wherein the higher concentration layer and the lower concentration layer are provided in an alternate and periodic manner, the repetition number of said higher concentration layer and said lower concentration layer is 10 to 1000 and a thickness of a repetition cycle is 1 nm to 1000 nm.

38. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the number of pits formed is in the range of $1 \times 10^5/cm^2$ to $1 \times 10^{10}/cm^2$.

39. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the flatness (Ra) of the surface of the lower concentration layer (a surface remote from the substrate) is not more m 10 angstroms.

40. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the thickness of the higher concentration layer and the thickness of the lower concentration layer each are 0.5 to 500 nm.

41. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the thickness of the lower concentration layer is equal to or larger than the thickness of the higher concentration layer.

42. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the thickness of the n-type impurity concentration periodic variation layer is 0.1 to 10 μm.

43. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the concentration of the n-type impurity in the higher concentration layer is 5×10^{17} to 5×10^{19} cm^{-3}.

44. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the concentration of the n-type impurity in the lower concentration layer is lower than the concentration of the n-type impurity in the higher concentration layer and is not more than 2×10^{19} cm^{-3}.

45. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 44, wherein the n-type impurity is not intentionally doped into the lower concentration layer.

46. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, which comprises a base layer, having a lower carrier concentration than the n-type impurity concentration periodic variation layer, between said substrate and said n-type impurity concentration periodic variation layer.

47. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 46, wherein said base layer contains an n-type impurity as a dopant and the concentration of the n-type impurity is not more than 5×10^{18} cm^{-3} .

48. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 47, wherein said base layer is undoped.

49. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 46, wherein the thickness of the base layer is not less than 1 μm and not than 20 μm.

50. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 49, wherein the thickness of the base layer is not less than 5 μm and not more than 15 μm.

51. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 46, wherein the carrier concentration of the base layer is not more than 5 x 10^{17} cm^{-3}.

52. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 37, wherein the plane direction of the surface of the substrate is slightly inclined with respect to the just direction.

53. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 52, wherein the plane direction of the surface of the substrate is inclined by 0.05 to 0.6 degree with respect to the just direction.

54. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 52 wherein said substrate is selected from the group consisting of oxide single crystal materials such as sapphire (α-Al_2O_3 single crystal), zinc oxide (ZnO), and gallium lithium oxide ($LiGaO_2$) , group IV semiconductor single crystals including silicon (Si) single crystals (silicon) and cubic or hexagonal silicon carbide (SiC), and group III-V compound semiconductor single crystals including gallium phosphide (GaP), gallium arsenide (GaAs), and gallium nitride (GaN).

55. (currently amended): A process for producing a n-type group III nitride semiconductor layered structure, which layered structure comprises ~~comprising~~ a substrate and an n-type impurity concentration periodic variation layer stacked on the substrate, the variation layer comprising an n-type impurity atom higher concentration layer and an n-type impurity atom lower concentration layer; wherein said n-type impurity atom is Ge, wherein pits are provided on a surface of the higher concentration layer remote from the substrate, wherein said lower concentration layer is stacked on said higher concentration layer, and wherein the higher concentration layer and the lower concentration layer are provided in an alternate and periodic manner where the repetition number of said higher concentration layer and said lower concentration layer is a number from 10 to 1000 and a thickness of a repetition cycle is 1 nm to 1000 nm,

which process comprises stacking~~wherein~~ each of said n-type impurity atom higher concentration layer and said n-type impurity atom lower concentration layer ~~is stacked~~ so that, in addition to the concentration of the n-type impurity to be doped, conditions for growth within a reactor are also differentiated.

56. (previously presented): The process according to claim 55 wherein conditions for growth of the lower concentration layer are differentiated from conditions for growth of the higher concentration layer so that two-dimensional growth of the layer is accelerated during the growth of the lower concentration layer.

57. (previously presented): The process according to claim 55, wherein the lower concentration layer is grown at a temperature different from the temperature at which the higher concentration layer is grown.

58. (previously presented): The process according to claim 57, wherein the lower concentration layer is grown at a temperature above the temperature at which the higher concentration layer is grown.

59. (previously presented): The process according to claim 55, wherein the lower concentration layer is grown at a pressure different from the pressure at which the higher concentration layer is grown.

60. (previously presented): The process according to claim 59, wherein the lower concentration layer is grown at a pressure lower than the pressure at which the higher concentration layer is grown

61. (previously presented): The process according to claim 55, wherein the carrier gas flow rate in the growth of the lower concentration layer is different from the carrier gas flow rate in the growth of the higher concentration layer.

62. (previously presented): The process according to claim 61, wherein the carrier gas flow rate in the growth of the lower concentration layer is higher than the carrier gas flow rate in the growth of the higher concentration layer.

63. (previously presented): The process according to claim 55, wherein the growth speed of the lower concentration layer is different from the growth speed of the higher concentration layer.

64. (previously presented): The process according to claim 63, wherein the growth speed of the lower concentration layer is lower than the growth speed of the higher concentration layer.

65. (previously presented): The process according to claim 55, wherein the nitrogen/III ratio in the growth of the lower concentration layer is different from the nitrogen/III ratio in the growth of the higher concentration layer.

66. (previously presented): The process according to claim 65, wherein the nitrogen/III ratio in the growth of the lower concentration layer is lower than the nitrogen/III ratio in the growth of the n-type impurity atom higher concentration layer.

67. (withdrawn): A group III nitride semiconductor light-emitting device comprising a light-emitting layer composed of a group III nitride semiconductor provided on the substrate, wherein the n-type group III nitride semiconductor layered structure according to claim 37 is provided between the substrate and the light-emitting layer.

68. (withdrawn): The n-type group III nitride semiconductor layered structure according to claim 53 wherein said substrate is selected from the group consisting of oxide single crystal materials such as sapphire (α-Al_2O_3 single crystal), zinc oxide (ZnO), and gallium lithium oxide ($LiGaO_2$) , group IV semiconductor single crystals including silicon (Si) single crystals (silicon) and cubic or hexagonal silicon carbide (SiC), and group III-V compound semiconductor single crystals including gallium phosphide (GaP), gallium arsenide (GaAs), and gallium nitride (GaN).